SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
Siddharth Nagar, Narayanavanam Road – 517583
QUESTION BANK

Subject with Code : MICROPROCESSORS AND MICROCONTROLLERS (20EC0416)
Course & Branch : B.Tech – EEE **Year & Sem:** III &II **Regulation:** R20

UNIT–I
MICROPROCESSORS, MICROCOMPUTERS AND ASSEMBLY LANGUAGE

1.	a)	Draw the block diagram of a computer and explain the function of each block.	**[L2] [CO2]**	**[6M]**
	b)	Draw the block diagram of a computer with microprocessor as CPU and explain each block.	**[L2] [CO2]**	**[6M]**
2.	a)	Describe microprocessor based system with bus architecture	**[L1] [CO2]**	**[6M]**
	b)	Summarize the sequence of steps how the microprocessor works	**[L2] [CO1]**	**[6M]**
3.	a)	Classify the computer languages and describe each	**[L2] [CO2]**	**[6M]**
	b)	Compare the computer languages	**[L2] [CO1]**	**[6M]**
4.	a)	Write the functions of the following A) Assembler B) Compiler C) Interpreter	**[L1] [CO2]**	**[6M]**
	b)	Discuss the development of computers	**[L2] [CO1]**	**[6M]**
5.	a)	Summarize the applications mainframes, workstations and single board microcomputers	**[L2] [CO1]**	**[6M]**
	b)	Explain microprocessor based temperature system with neat Diagram	**[L4] [CO1]**	**[6M]**
6.	a)	Discuss the microprocessor initiated operations	**[L2] [CO2]**	**[6M]**
	b)	Recall the functions of different Busses in the bus organization	**[L1] [CO1]**	**[6M]**
7.	a)	Classify the memories and discuss each	**[L2] [CO2]**	**[6M]**
	b)	Give the details of Latch and tri-state buffer with neat diagrams	**[L4] [CO2]**	**[6M]**
8.	a)	Draw the memory address map diagram to interface for 512 bytes from 8000 location	**[L3] [CO1]**	**[6M]**
	b)	Discuss the following memory models A) RAM B) ROM.	**[L2] [CO2]**	**[6M]**
9.	a)	Describe the following memories A) Static RAM B) Dynamic RAM.	**[L2] [CO2]**	**[6M]**
	b)	Discuss the following A) PROM B) EPROM C) EEPROM.	**[L2] [CO2]**	**[6M]**
10.	a)	Review the I/O devices identification methods	**[L2] [CO2]**	**[6M]**
	b)	Explain microcomputer systems	**[L2] [CO1]**	**[6M]**

1.	**The physical components of the system is known as**				**[ ]**
	A)Hardware	**B) Software**	**C)Program**	**D)Memory**	
2.	**A set of instructions written for the microprocessor to perform a task is called** **A) Program B) Hardware C) Software D)Memory**				**[ ]**
3.	**Group of programs is called** **A) Software B) Hardware C)Program D)Memory**				**[ ]**
4.	**Each processor recognize and process a group of bits called** **A) Word B) Byte C)Nibble D)Bit**				**[ ]**
5.	**LSI means** **A) Large scale Integration B) Low scale integration Software** **C) Level scale integration D) None**				**[ ]**
6.	**Group of 8 bits is called** **A) Byte B) Nibble C) Word D) Bit**				**[ ]**
7.	**Group of 4 bits is called** **A) Nibble B) Byte C) Word D) Bit**				**[ ]**
8.	**The Program written in Mnemonics is called____ Language program** **A)Assembly B) Machine C) High Level D)None**				**[ ]**
9.	**The Program written in Binary is called____ Language program** **A)Machine B) Assembly C) High Level D)None**				**[ ]**
10.	**The Program written in C, Fortran, Java is called____ Language program** **A) High Level B) Assembly C) Assembly D)None**				**[ ]**
11.	**Low level languages are** **A)Machine B) Assembly C) Both D) None**				**[ ]**
12.	**The program which translates mnemonics to machine code is called** **A) Assembler B) compiler C)Interpreter D)None**				**[ ]**
13.	**The ------ translates the source code into machine language** **A)Compiler B) Assembler C) Machine D)None**				**[ ]**
14.	**The ------ translates one statement at a time from the source code into machine language** **A)Interpreter B) Assembler C) Machine D) Compiler**				**[ ]**

15.	**The _____ computers have high speed and high word length.** **A) Mainframe B) Personal C)Microcomputer D)Single chip**	**[ ]**
16.	**The _____ computers are used for CAD, CAE and CAM applications** **A) Workstations B) Personal C)Microcomputer D)Single chip**	**[ ]**
17.	**The _____ microcomputers are used for college laboratories and industries** **A) Single Board B) Personal C) Workstations D) Single chip**	**[ ]**
18.	**The logic design of the microprocessor is called -----** **Architecture B) Software C) Program D)Memory**	**[ ]**
19.	**The Busses present in processor are ___** **A) Address B) Data C)Control D) All**	**[ ]**
20.	**_____ Bus is unidirectional** **A) Address B) Data C) Both D) None**	**[ ]**
21.	**_____ Bus is Bidirectional** **A) Data B) Address C) Both D) None**	**[ ]**
22.	**If microprocessor is having 12 address lines then it can address _____ memory locations** **A) 4K B) 8K C) 1K D) None**	**[ ]**
23.	**If microprocessor address 16K byte memory then required address lines are** **A) 14 B) 8 C) 16 D) None**	**[ ]**
24.	**In a 32 bit processor the size of data bus is** **A) 32 B) 64 C) 16 D) None**	**[ ]**
25.	**Memory Read is a _____ signal** **A) Control B) Data C) Address D)None**	**[ ]**
26.	**I/O Read is a _____ signal** **A) Control B) Data C) Address D)None**	**[ ]**
27.	**The memory addresses assigned to a memory chip is called** **A) Memory map B) Data Map C) Control Map D) None**	**[ ]**
28.	**Basic element of memory is _____** **A) Flip-flop B) Adder C) Nand gate D) None**	**[ ]**
29.	**ROM is ---** **A) Read Only Memory B) Random only Memory C) Read once memory D) None**	**[ ]**
30.	**Secondary memory is _____.**	**[ ]**

	A) Hard disk B) RAM C) ROM D) None	
31.	**Primary Memory is** **A) RAM B) Hard Disk C) Floppy Disk D) None**	**[ ]**
32.	**Static Memory is made up of _____** **A) Flip-flops B) Transistors C) Oscillators D) None**	**[ ]**
33.	**Dynamic Memory is made up of _____** **A) Transistors B) Flip-flop C) Oscillators D) None**	**[ ]**
34.	**RAM is _____memory** **A) Volatile B) Non Volatile C) Not Erasable D) None**	**[ ]**
35.	**Refreshing circuit require in _____memory** **A) DRAM B) SRAM C) PROM D) None**	**[ ]**
36.	**ROM is _____memory** **A) Non-Volatile B) Volatile C) Not readable D) None**	**[ ]**
37.	**The EEPROM erases the data at _____level** **A) Register B) Block C) Sector D) None**	**[ ]**
38.	**In Peripheral mapped I/O the I/Os are with _____ bit address** **A) 8 B) 16 C) 32 D) None**	**[ ]**
39.	**In Memory Mapped I/O the I/Os are with _____ bit address** **A) 16 B) 8 C) 32 D) None**	**[ ]**
40.	**The latch, Buffers and bus drivers are known as _____ Devices** **A) Interfacing B) Storage C) Addressing D) None**	**[ ]**

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UNIT–II
8085 MICROPROCESSOR ARCHITECTURE

1.	a)	Give the details of 8085 microprocessor	**[L3] [CO2]**	**[6M]**
	b)	Draw a signal diagram of 8085	**[L3] [CO2]**	**[6M]**
2.	a)	Define multiplexing of the Bus .Explain multiplexed data and address in 8085.	**[L3] [CO2]**	**[6M]**
	b)	Discuss the control signals in 8085.	**[L3] [CO1]**	**[6M]**
3.	a)	Describe the interrupts in 8085.	**[L3] [CO2]**	**[6M]**
	b)	Review the following signals A) HOLD B) HLDA C) READY	**[L3] [CO1]**	**[6M]**
4.	a)	Recognize the importance of the following signals A) ALE B) INTR C) INTA	**[L3] [CO2]**	**[6M]**
	b)	With neat diagram explain the microprocessor communication with memory	**[L3] [CO1]**	**[6M]**
5.	a)	With neat diagram explain demultiplexing the bus AD7-AD0	**[L3] [CO1]**	**[6M]**
	b)	Draw the architecture of 8085	**[L3] [CO1]**	**[6M]**
6.	a)	Explain different blocks in 8085 architecture	**[L3] [CO2]**	**[6M]**
	b)	List and discuss flags in 8085	**[L3] [CO1]**	**[6M]**
7.	a)	With example explain one , two and three byte instructions	**[L4] [CO2]**	**[6M]**
	b)	Determine the different ways of specifying the data in the instruction.	**[L4] [CO2]**	**[6M]**
8.	a)	Give the classification of instruction set and any 2 examples in each set	**[L4] [CO1]**	**[6M]**
	b)	Give the function of the following instructions A) LXI B) SBI C) POP D) JPO E) DI F) XCHG	**[L4] [CO2]**	**[6M]**
9.	a)	Calculate the result in A and B registers after executing each of the instructions with initial values of A=56, B=37 And Carry bit is 1. A) ADD B B) SBB B C) XRA B	**[L4] [CO2]**	**[6M]**
	b)	Describe the function of the following instructions A) OUT B) MOV C) XRA D) RLC E) PUSH F) CALL	**[L4] [CO2]**	**[6M]**
10.	a)	Calculate the result in A and B registers and carry flag condition after executing each of the following instructions with initial values of A=96, B=82 and Carry bit is 0. A) MOV A,B B) ADD B C) ANA B	**[L4] [CO2]**	**[6M]**
	b)	Discuss the function of the following instructions A) CMA B) IN C) NOP D) HLT E) JC F) ADI	**[L4] [CO1]**	**[6M]**

1.	**The 8085 is ____ bit processor** **A) 8 B) 16 C) 4 D) 20**	**[ ]**
2.	**The 8085 have____ bit address bus** **A) 16 B) 8 C) 4 D) 20**	**[ ]**
3.	**The 8085 can address _____ of memory** **A) 64K B) 8K C) 4K D) 20K**	**[ ]**
4.	**_____ address lines are multiplexed with data bus in 8085** **A) Lower B) Higher C) Both D) None**	**[ ]**
5.	**$IO/\overline{M}$ =0 and $\overline{Rd}$=1 and $\overline{WR}$=0 the microprocessor is doing____ operation** **A) Memory write B) Memory Read C) IO Read D)None**	**[ ]**
6.	**$IO/\overline{M}$ =1 and $\overline{Rd}$=0 and $\overline{WR}$=1 the microprocessor is doing** **A) IO Read B) Memory Read C) IO Write D)None**	**[ ]**
7.	**ALE means_____** **A) Address Latch Enable B) Address low enable C) Add latch enable D) Bit**	**[ ]**
8.	**Higher priority interrupt is ____** **A) RST7.5 B) RST6.5 C) RST5.5 D) INTR**	**[ ]**
9.	**The non MASKABLE Interrupt is___** **A) TRAP B) RST6.5 C) RST5.5 D) INTR**	**[ ]**
10.	**Direct Memory Access signal is** **A) HOLD B) SID C) INTR D)TRAP**	**[ ]**
11.	**HOLD acknowledgement signal is** **A) HLDA B) INTA C) HOAA D) None**	**[ ]**
12.	**The program counter is zero when ____ signal goes low** **A) RESET IN B) RESET OUT C) INTA D)HLDA**	**[ ]**
13.	**_____ signal is used for demultiplexing the address and data** **A) ALE B) SOD C) TRAP D) DLE**	**[ ]**
14.	**The number of control signals required to communicate with memory and IO** **A) 4 B) 5 C) 6 D) 8**	**[ ]**
15.	**Number of 8bit general purpose registers in 8085** **A) 7 B) 10 C) 12 D) 20**	**[ ]**
16.	**The 16bit registers are**	**[ ]**

	A) PC and SP B) PC and A C) SP and B D) D and H	
17.	**The Sign bit is 1 if the result is** **A) Negative B) Positive C) Both A&B D) Neither A or B**	**[ ]**
18.	**AC flag is set when there is a carry from ___ bit to ____bit** **A) D3 to D4 B) D4 to D5 C) D6 to D7 D) Do to D1**	**[ ]**
19.	**Number of flags in 8085 are ___** **A) 5 B) 6 C) 7 D) 8**	**[ ]**
20.	**when the instruction is fetched from memory it is placed in ___ register** **A) Instruction B) Program counter C) Stack Pointer D) None**	**[ ]**
21.	**Task to be performed is given as _____** **A) Opcode B) Operand C) Control D) None**	**[ ]**
22.	**The data to be operated on is called _____** **A) Operand B) Opcode C) Control D) None**	**[ ]**
23.	**ADD B is ____ byte instruction** **A) 1 B) 2 C) 3 D) 4**	**[ ]**
24.	**ADI 25H is ____ byte instruction** **A) 2 B) 1 C) 3 D) 4**	**[ ]**
25.	**LDA 2050 is ____ byte instruction** **A)3 B) 2 C) 1 D) 4**	**[ ]**
26.	**The various ways of specifying the data in the instruction is called ____ Modes** **A) Addressing B) Data C) Control D)None**	**[ ]**
27.	**BCD stand for** **A) Binary Coded Decimal B) Binary code decimal C) Base Coded Decimal D) None**	**[ ]**
28.	**ASCII is ____ bit Code** **A) 7 B) 8 C) 9 D) 10**	
29.	**BCD numbers ranges from ---** **A) 0 to 9 B) 0 to A C) 0 to F D) 0 to 8**	**[ ]**
30.	**The largest unsigned number processed by 8085 is ____** **A) FF B) AA C) 99 D) None**	**[ ]**
31.	**An 8 bit register can accommodate ___ number of BCD digits** **A) 2 B) 3 C) 4 D) 5**	**[ ]**

32.	**Which of the following is not a data transfer instruction _____** **A) ADI B) LXI C) MOV D) STAX**	**[ ]**
33.	**Which of the following is not a register pair** **A) A&B B) B&C C) D&E D) H&L**	**[ ]**
34.	**In the instruction OUT 8bit the 8 bit indicates _____ Address** **A) Port B) Register C) Interrupt D) Data**	**[ ]**
35.	**MOV A,M copy the data from address specified by___ register pair** **A) H&L B) B&C C) D&E D) A&B**	**[ ]**
36.	**XRA A is results _____** **A) A=00 B) A=01 C) A=FF D) None**	**[ ]**
37.	**JNZ checks ____ Flag** **A) Zero B) Parity C) Sign D) None**	**[ ]**
38.	**JMP checks ____ Flag** **A) Zero B) Parity C) Sign D) None**	**[ ]**
39.	**PUSH and POP instructions uses ____** **A) Stack pointer B) Program Counter C) Accumulator D) None**	**[ ]**
40.	**STC sets _____ Flag** **A) Carry B) Zero C) Sign D) None**	**[ ]**

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UNIT – III

The 8051 Architecture

1.	a)	List the features of 8051 microcontroller.	**[L1] [CO3]**	**[6M]**
	b)	Differentiate Microprocessor and Microcontroller.	**[L2] [CO2]**	**[6M]**
2.	a)	Draw the internal architecture of 8051 microcontroller.	**[L3] [CO3]**	**[6M]**
	b)	Explain the function of each block in 8051 microcontroller.	**[L2] [CO3]**	**[6M]**
3.	a)	Draw the pin diagram of 8051 microcontroller.	**[L3] [CO3]**	**[6M]**
	b)	Describe the functionality of following pins. i) RXD ii) INT iii) T0 iv) PSEN v) EA vi) ALE	**[L2] [CO3]**	**[6M]**
4.	a)	Explain the following registers. i) Program Counter ii) Data Pointer	**[L2] [CO3]**	**[6M]**
	b)	Review the PSW Register in 8051 microcontroller.	**[L1] [CO3]**	**[6M]**
5.	a)	Discuss how the Internal RAM memory is organized in 8051 microcontroller.	**[L2] [CO3]**	**[6M]**
	b)	Discuss different Functions of ports.	**[L2] [CO3]**	**[6M]**
6.	a)	Explain about Timer/counter control logic in 8051 with diagram.	**[L2] [CO4]**	**[6M]**
	b)	Discuss the TCON Special Function Register.	**[L2] [CO3]**	**[6M]**
7.	a)	Explain the role of each bit in TMOD Register.	**[L2] [CO3]**	**[6M]**
	b)	Give the details of timer mode 0 & mode1.	**[L2] [CO3]**	**[6M]**
8.	a)	Discuss the Auto Reload mode in the 8051 microcontroller.	**[L2] [CO3]**	**[6M]**
	b)	Explain the different serial data transmission modes in 8051.	**[L2] [CO3]**	**[6M]**
9.	a)	Describe how the serial communication modes are set using SCON, PCON register in 8051μC	**[L1] [CO3]**	**[6M]**
	b)	Explain how the 8051 microcontroller transfers the serial data in UART mode.	**[L2] [CO4]**	**[6M]**
10.	a)	Describe the IE and IP registers.	**[L1] [CO3]**	**[6M]**
	b)	List and discuss different types of interrupts in the 8051microcontroller.	**[L2] [CO3]**	**[6M]**

1.	_____are the processor chips that generally have memory, input ports and Output ports within the chip itself				[ ]
	A) Microcontroller	B) Microprocessor	C) NOC	D) None	
2.	8051 Crystal frequency is				[ ]
	A) 12MHZ	B) 5MHZ	C) 2MHZ	D) 10MHZ	
3.	Program Counter of 8051 is _____ bit register				[ ]
	A) 16 bit	B) 8 bit	C) 4 bit	D) 2 bit	
4.	8051 Data Pointer is _____ bit register				[ ]
	A) 16 bit	B) 8 bit	C) 4 bit	D) 2 bit	
5.	8051 Internal RAM is of				[ ]
	A) 128 bytes	B) 120 bytes	C) 8 bytes	D) 64 bytes	
6.	Number of Register banks in 8051				[ ]
	A) 4	B) 3	C) 2	D) 8	
7.	Number of I/O ports in 8051				[ ]
	A) 4	B) 3	C) 2	D) 8	
8.	Port P0 has _____number of pins				[ ]
	A) 8	B) 4	C) 2	D) 6	
9.	Number of pins in 8051				[ ]
	A) 40	B) 30	C) 20	D) 8	
10.	The 8051 contains _____ 16-bit registers				[ ]
	A)2	B)3	C)4	D)5	
11.	The 8051 contains _____ general purpose or working registers				[ ]
	A) 34	B)32	C)16	D)8	
12.	_____ are 1-bit registers provided to store the results of certain program instructions				[ ]
	A) Flags	B) Tags	C)Ports	D)Clocks	
13.	____ architecture uses the same address in different memories, for code and data				[ ]
	A) Hardvard	B) Von-Neuman	C)Both	D)None	
14.	The bit addressable area in RAM is_____				[ ]
	A) 20H to 2FH	B)00H to 1FH	C)30H to 3FH	D)10H to 20H	
15.	The RAM area above the bit addressable area that can addressable as bytes				[ ]
	A)30H to 7FH	B) 20H to 2FH	C) F0H to FFH	D) 00H to 3FH	
16.	The 8-bit register used to hold address of the top of the stack is called as_____				[ ]
	A) Stack Pointer	B) PSW	C)DPTR	D)TMOD	
17.	The 8051 internal RAM addresses from 80H to FFH are called				[ ]
	A) SFR	B) PSW	C)TCON	D)SBUF	
18.	The PC is used to address program code bytes from addresses _____				[ ]
	A)0000h to FFFFh	B)00FFh to FFFFh	C)100Fh to 0FFFh	D)8080h to F0F0h	
19.	___ Port is used as a bidirectional low-order address and data bus for external memory.				[ ]
	A) Port 0	B) Port 1	C)Port 2	D)Port 3	
20.	_____port is used to supply a high order address byte				[ ]
	A) Port 2	B) Port 3	C)Port 0	D)Port 1	
21.	_____ register is needed to access external RAM				[ ]
	A) DPTR	B) PC	C) PSW	D) TMOD	
22.	Timer modes are set using ____register				[ ]

	A) TMOD	B) TCON	C) SBUF	D) SCON	
23.	Number of timers in 8051				[ ]
	A) 2	B) 3	C) 4	D) 8	
24.	The timer counts the 8051 oscillator's internal clock frequency divided by				[ ]
	A) 12	B) 8	C)16	D) 32	
25.	Based on M1 and M0, Timers in _____ number of modes.				[ ]
	A) Four	B) Three	C) One	D) None	
26.	_____ flag is set when timer 1 overflows				[ ]
	A) TF1	B) TF0	C) IT1	D) IT0	
27.	_____ signal used to run or stop the timer.				[ ]
	A) GATE	B) IT1	C) C/T	D) IE1	
28.	___ bit is set to 1 to make timer acts as a counter.				[ ]
	A) C/T	B) Gate	C) M1	D) M0	
29.	In mode 0 the THX register and TLX is act as a ___bit counters respectively.				[ ]
	A) 8,5	B) 8,8	C) 5,8	D) 8,16	
30.	In _____mode only TLX counter as an 8-bit counter.				[ ]
	A) 2	B) 1	C) 0	D) 3	
31.	_____ register is used to hold the data for serial data communication in 8051				[ ]
	A) SBUF	B) SCON	C) PCON	D) TCON	
32.	Number of programmable modes for serial data communication.				[ ]
	A) 4	B) 6	C) 5	D) 8	
33.	SM0=0, SM1=0 then the 8051 transfer the data as				[ ]
	A) Shift Register	B) 8 bit UART	C) 9 bit UART	D) None	
34.	_____ bit of PCON register is set to 1 to double baud rate.				[ ]
	A) SMOD	B) GF1	C) GF0	D) PD	
35.	The bit of PCON register used to enter power down configuration is _____				[ ]
	A) PD	B) SMOD	C) IDL	D) GF1	
36.	Reception of serial data will begin if the ___ bit in SCON is set to 1 for all modes				[ ]
	A) REN	B) TB8	C) RB8	D) TI1	
37.	SM0 and Sm1 in SCON to____ configures SBUF to receive or transmit 8 data bits				[ ]
	A) 00b	B) 01b	C) 10b	D)11b	
38.	___interrupts are provided in the 8051				[ ]
	A) 5	B) 6	C) 7	D) 8	
39.	When a high level is applied to the ___ pin, the 8051 enters a reset condition				[ ]
	A) RST	B) INT0	C) INT1	D)VCC	
40.	_____ register used to change the interrupts priority				[ ]
	A) IP	B) IE	C) SCON	D) TMOD	